A Balanced Distributed Preamplifier using MMIC GaAs MESFET Technology

T. L. Nguyen and A. P. Freundorfer

Department of Electrical and Computer Engineering
Queen's University
Kingston, Ontario
Canada K7L-3N6

Phone (613)545-2925
fax (613)545-6615
freund@eleceng.ee.queensu.ca

TH
2D

ABSTRACT

A MMIC balanced preamplifier was fabricated using a 0.8 μm gate length process. A 45 dBΩ transimpedance gain, a 6 GHz bandwidth, a $10 pA/\sqrt{Hz}$ input noise and a 12 dB CMRR were measured.

INTRODUCTION

Balanced receivers with large bandwidths can be used in intensity modulated (IM) lightwave systems or in continuous phase frequency shift keyed (CPFSK) lightwave systems. In the IM system, they can be used at the receiver to obtain a duobinary encoded signal at the preamplifier output [1]. In a coherent CPFSK system, the balanced receiver can improve the receiver sensitivity by 3 dB [2]. One can eliminate the local oscillator laser used in the coherent CPFSK system by using a Mach-Zehnder interferometer filter [3] and a balanced receiver to incoherently detect the CPFSK signal[4]. With data rates in excess of one gigabit per second, both IM and CPFSK lightwave systems will require large bandwidth preamplifiers that have associated problems of high frequency noise which increases as frequency squared (f^2) [2]. Most balanced receivers used in current research utilize dual photodiodes followed by an electronic preamplifier. There are several inherent disadvantages to this configuration. One disadvantage is that the resultant capacitance is doubled because of the two anti-parallel photodiodes. This leads to a reduction in bandwidth and an increase in high frequency noise [2]. A solution is to separate the photodiodes with their own preamplifier and then sum the signals at the output of the preamplifiers [5]. Off-the-shelf descrete components were used to demonstrate the method. A MMIC version of this balanced topology has never been reported and is presented here.

CIRCUIT DESIGN

The circuit representation of the balanced distributed (DA) preamplifier is shown in Fig. 1. The input and output parasitic capacitance of the transistors with the inductors create artificial

0-7803-3246-6/96/$5.00 © IEEE

transmission lines which have an inherently large bandwidth. Using high gate line impedance in DA will reduce the equivalent input noise [6]. Also note that since the photodiodes are connected in separate arms, the load capacitance seen by the preamplifier is half that of the dual diode single preamplifier case; hence a wide bandwidth can be obtained with improved noise performance. High frequency noise can also be reduced by using tuning networks [7]. The theory of general lossless filter was applied [8] to design the front-end tuning network. A fourth-order Tchebyshev filter was constructed to minimize noise between 2 GHz and 6 GHz. The filter type tuning network included the bondwire inductance, on chip inductor and capacitor, and the *p-i-n* photodiode capacitance. The bandwidth of the front-end is dictated not by the cut-off frequency (17 GHz) of the gate and drain lines, but by the tuning network (6 GHz). The preamplifier was simulated to have a midband transimpedance gain of 47 dBΩ, a bandwidth of 6 GHz, and an equivalent input noise current density of 10 $pA/\sqrt{Hz}$. A MMIC dual branch *p-i-n*-preamplifier using distributed amplification topology was fabricated using the Northern Telecom (NT) GaAs SAGRF 0.8 μm gate process and the layout is shown in Fig. 2. The equiripple passband of transimpedance gain in Fig. 3 is a result of the tuning network. The measured transimpedance gain and the input noise correspond well with the predicted results. The measured common mode rejection ratio (CMRR) is shown in Fig. 4. CMRR degrades drastically at 6 GHz. Back-simulation suggests that a major contribution to the degradation is a result of bond wire length mismatch. A 10% mismatch results in a CMRR response of 17 dB at 6 GHz.

CONCLUSION

A transimpedance gain of 45 dBΩ, a bandwidth of 6 GHz, an equivalent input noise current density of $10\,pA/\sqrt{Hz}$, and a CMRR of 12 dB were measured for the balanced preamplifier. The preamplifier was used in a 1 Gb/s coherent CPFSK system using a delay-and-multiply demodulator. The bit-error ratio vs. received optical power curve is plotted in Fig. 5. The receiver sensitivity is -43.2 dBm which is 7.5 dB away from the ideal shot-noise limit performance.

ACKNOWLEDGEMENTS

A special thanks goes to Chris Falt of BNR for his wire bonding expertise and M. Svilans of BNR for the photodiodes used in the experiment.

REFERENCES

[1] P.P. Smyth and B.R. White, "Optical detector," *IEEE Photon. Technol. Lett.*, vol. 5, no. 7, July 1995, pp. 239-240.

[2] G. Jacobsen, J. X. Kan, and I. Garrett, "Tuned front-end design for heterodyne optical receivers," *J. Lightwave Technol.*, vol. 7, no. 1, Jan. 1989, pp. 105-114.

[3] N. Takato *et al*, "Silica-based integrated optic Mach-Zehnder multi/demultiplexer family with channel spacing of 0.01-250nm," *IEEE J. Select. Areas Commun.*, vol. 8, no. 6, Aug. 1990, pp. 1120-1127.

[4] H. Toba, K. Oda, and K. Nosu, "Design and performance of FSK-direct detection scheme for optical FDM systems," *J. Lightwave Technol.*, vol. 9, no. 10, Oct. 1991, pp. 1335-1343.

[5] P. W. Hooijmans, M. T. Tomesen, and A. van de Grijp, "A 2.3 Ghz low noise balanced receiver for FSK heterodyne reception, using commercially available component," 15th Europian Conf. on Opt. Comm., ECOC'89, Gotenburg, Sweden, Sept. 1989, pp. 392-395.

[6] A. P. Freundorfer and P. X. Lionais, "A low-noise broad-band GaAs MESFET monolithic distributed preamplifier," *IEEE Photon. Technol. Lett.*, vol. 7, no. 4, April 1995, pp. 424-426.

[7] J. L. Gimlett, "Low-noise 8 GHz PIN/FET optical receiver," *Elect. Lett.*, vol. 23, no. 6, Mar. 1987, pp. 281-283.

[8] G. Matthaei, L. Young and E.M.T. Jones, " Microwave filters, impedance-matching networks, and coupling structures," Artech House, 1980, pp. 104-112.

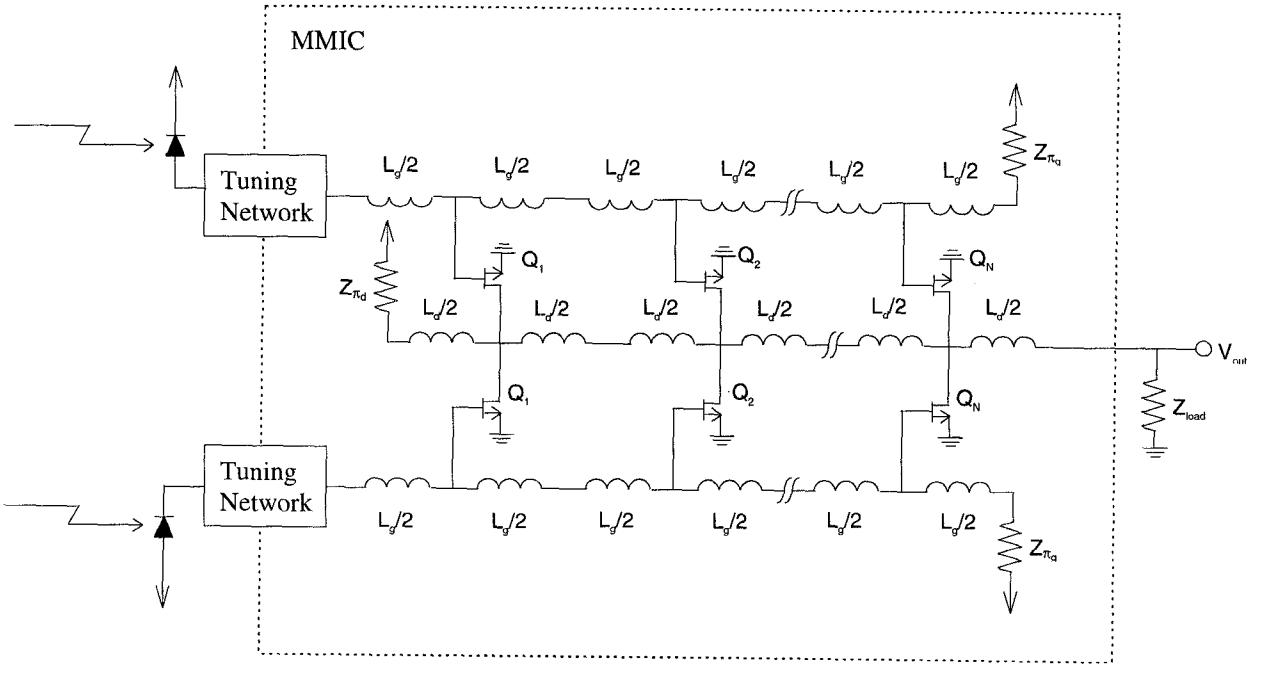

Figure 1 - Balanced distributed preamplifier circuit diagram.

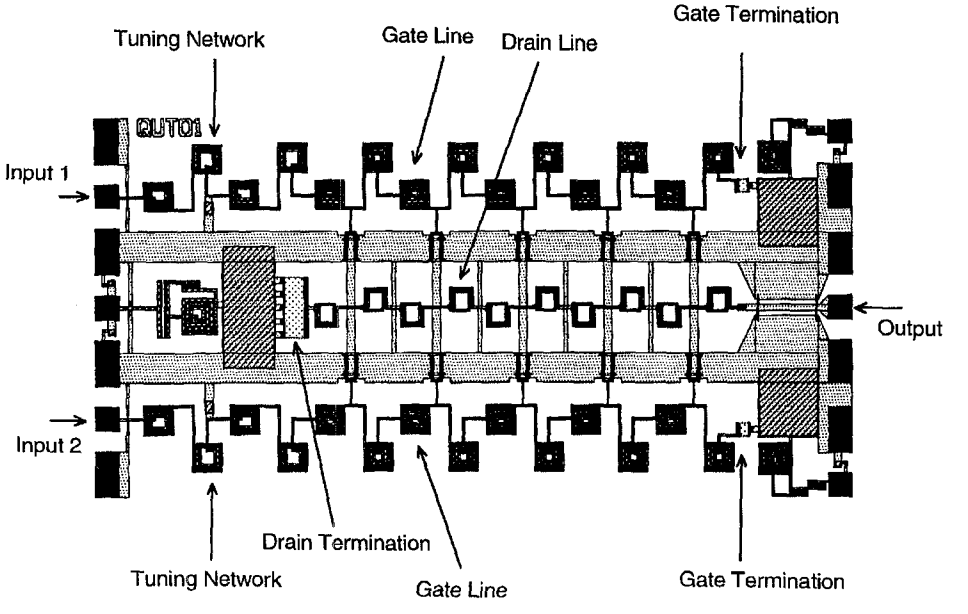

Fig. 2 Layout of balanced preamplifier chip

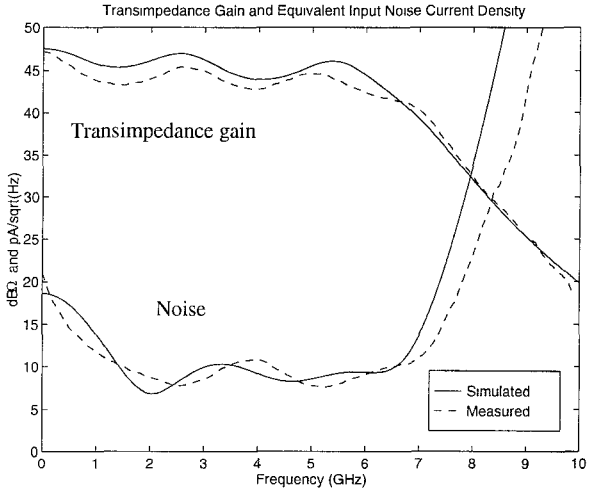

Figure 3 - Transimpedance and noise response.

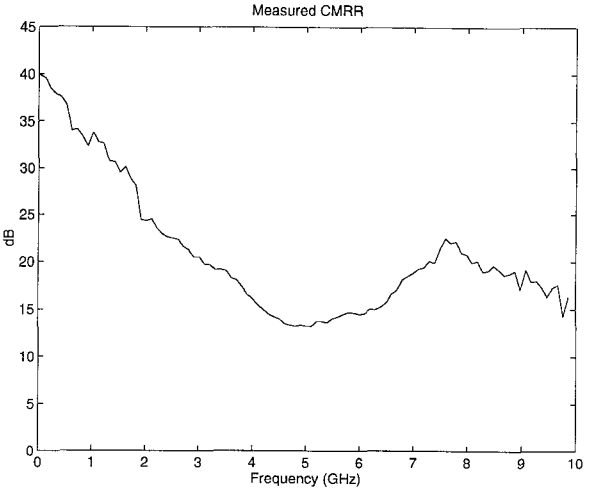

Figure 4 - CMRR versus frequency.

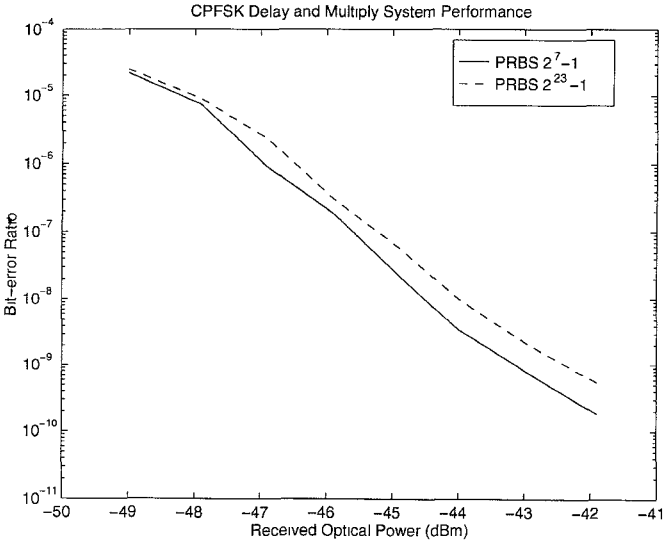

Figure 5 - Coherent CPFSK System performance at 1Gb/s.